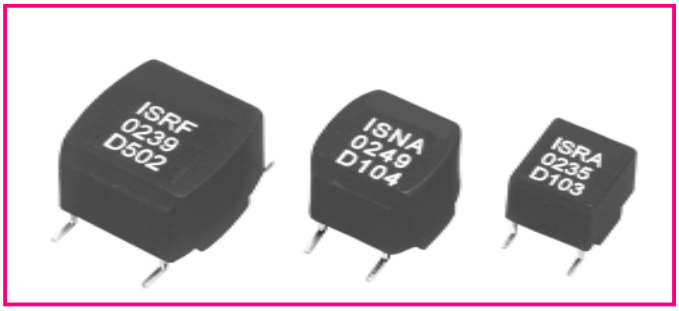
Pulse Transformers for SMD-Assemblies

IS Series, Turns Ratio 1:1, 2:1 and 1:1:1

Voltage time integral U_s x T_w: 150 - 400 Vµs
Pulse rise time T_r: 0.05 - 1.5 µs
Working voltage: $U_{eff} \leq$ 600 VAC
Partial discharge voltage: $U_e \leq 1.5 \times U_{eff}$
Climatic category: 25/100/21 acc. to IEC 60068-1
Plastic case: UL 94 V-0
Potting resin: UL 94 V-0



TIMONTA pulse transformers have been specially developed for the control of semi-conductors in power electronics.
Application possibilities are numerous and various and deal mainly with triggering Thyristors, Triacs, power transistors and IGBTs.
In most cases there is a suitable model available from the balanced component series for the development of dependable and economical circuits.

The desired specifications are archived through specifically selected materials and well-developed winding technology, and provide the following advantages:

- Electrical separation of circuit and power circuit, with a high insulation rating of at least 3.2 kV between the primary and secondary windings.
- Electrical separation with high insulation rating (at least 500 V) between secondary windings.
- Simple circuit layout, since there is sufficient power available to the circuit. This makes special extra provision on the power supply side unnecessary.
- Small coupling capacitances between primary and secondary windings limit transient feedback from the power supply side to the control electronics.
- The defined partial discharge voltage guarantees an effectively unlimited serviceable life.

Technical Data

Description	∫Udt [Vµs]	T_r [µs]	R_L [Ω]	I_t [A]	R_P [Ω]	R_S [Ω]	C_c [pF]	U_{isol} [kV~]	P_m(1) [W]	Case	Turn ratio [N]	L_s [mH]	Application
ISNA-0235-D103	200	0.9	100	0.1	1	1	20	3.5	0.5	35 - 3S	1 : 1	2.8	Universal
ISRA-0235-D103	200	0.05	100	0.1	1.5	1	80	3.2	0.5	35 - 3S	1 : 1	2.8	$T_R \leq 0.05$ µs
ISNA-0249-D104	300	1	100	0.1	0.7	0.7	20	3.5	0.7	49 - 3S	1 : 1	3.5	Universal
ISRA-0249-D104	300	0.05	100	0.1	0.7	0.7	90	3.2	0.7	49 - 3S	1 : 1	3.5	$T_R \leq 0.05$ µs
ISNA-0239-D202	400	1	60	0.17	0.4	0.4	20	3.5	1.0	39 - 3S	1 : 1	2.2	Universal
ISRA-0239-D502	400	0.1	20	0.5	0.4	0.4	100	3.2	1.0	39 - 3S	1 : 1	2.2	$T_R \leq 0.1$ µs
ISNB-0249-D101	250	1	100	0.1	1.0	0.5	20	3.5	0.7	49 - 3S	2 : 1	1.6	Universal
ISRB-0249-D101	250	0.05	100	0.1	1.0	0.5	70	3.2	0.7	49 - 3S	2 : 1	1.4	$T_R \leq 0.05$ µs
ISNB-0239-D202	350	1.5	60	0.17	0.8	0.4	20	3.5	1.0	39 - 3S	2 : 1	1.8	Universal
ISRB-0239-D502	350	0.5	20	0.5	0.8	0.4	90	3.2	1.0	39 - 3S	2 : 1	1.8	$T_R \leq 0.5$ µs
ISNF-0135-D101	150	0.9	100	0.1	0.5	0.5	10	3.5	0.5	35 - 4S	1 : 1 : 1	1.1	Universal
ISRF-0235-D101	150	0.05	100	0.1	1	0.5	40	3.2	0.5	35 - 4S	1 : 1 : 1	1.1	$T_R \leq 0.05$ µs
ISNF-0249-D101	250	1	100	0.1	0.5	0.5	20	3.5	0.7	49 - 4S	1 : 1 : 1	1.4	Universal
ISRF-0249-D101	250	0.05	100	0.1	0.4	0.5	70	3.2	0.7	49 - 4S	1 : 1 : 1	1.2	$T_R \leq 0.05$ µs
ISNF-0239-D202	350	1.5	60	0.17	0.4	0.4	20	3.5	1.0	39 - 4S	1 : 1 : 1	1.6	Universal
ISRF-0239-D502	350	0.5	20	0.5	0.4	0.4	90	3.2	1.0	39 - 4S	1 : 1 : 1	1.6	$T_R \leq 0.5$ µs

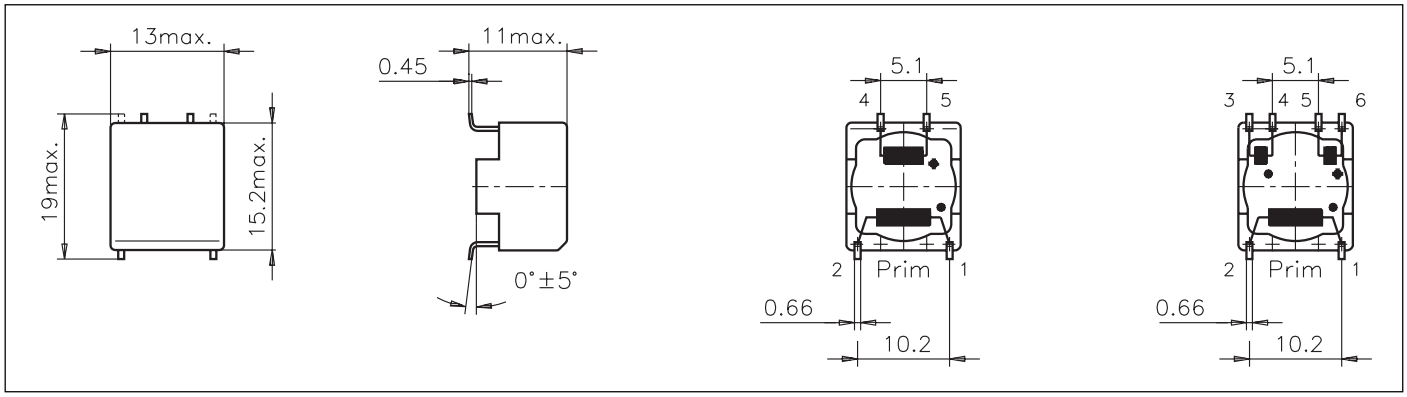
Table data at ϑa 25°C

(1) P_m@ ϑa 50°C; Power derating over 50°C: P= P_m x (100 -ϑa) / 50

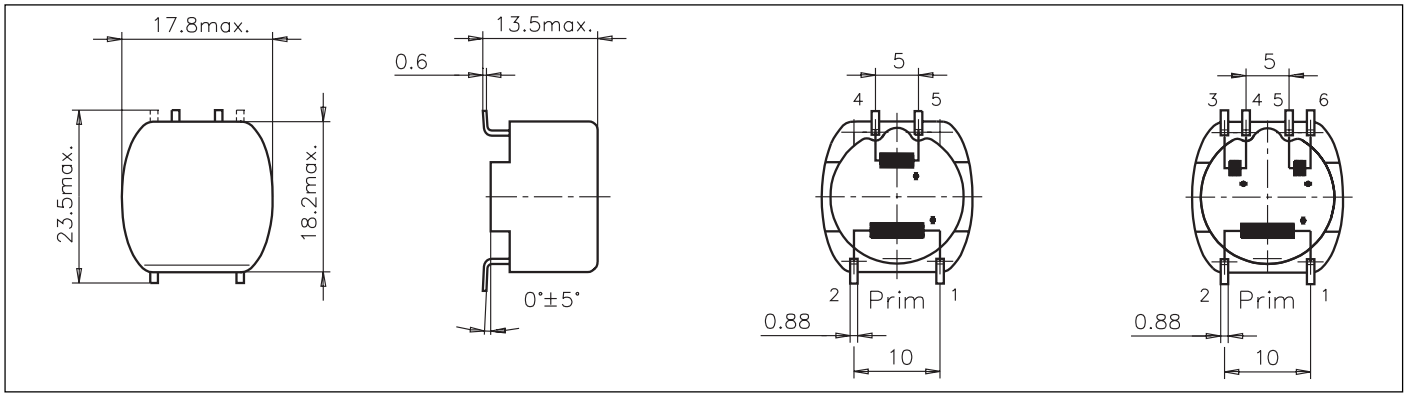
On request, models with other turn ratios are available.

Case for SMD mounting

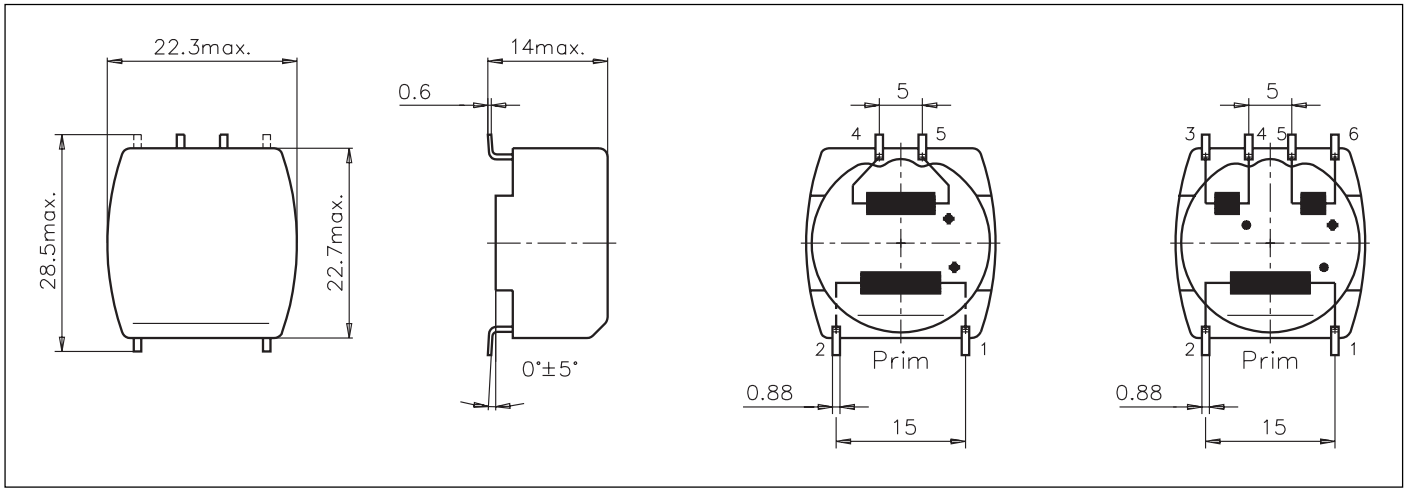
Case 35S **35-3S** **35-4S**



Case 49S **49-3S** **49-4S**



Case 39S **39-3S** **39-4S**



Possible solder land pattern for SMD mounting

Case 35S **49-S** **39-S**